Quiz Questions for: Name: ____________________________

Quiz 4: Ashenden 1.4-1.5,2.1.3 – Modeling/Introduction to Verilog

1. What does a Verilog module define?
2. What information is specified for each port in a Verilog module?
3. What is a structural model?
4. What is an instance?
5. What are the 2 forms for comments in Verilog?
6. What is a behavioral model?
7. What is synthesis?
8. Write a Verilog assignment statement to model the Boolean equation \( f = a \cdot \bar{b} + \bar{c} \).
9. What are the Verilog operators for the Boolean AND, OR, and NOT
10. How is a NAND written in Verilog?
11. Why should we generally not try to optimize Boolean equations manually when modeling them in Verilog?